FIG. 1

SEMICONDUCTOR MEMORY DEVICE
ACCORDING TO FIRST EMBODIMENT OF THE INVENTION

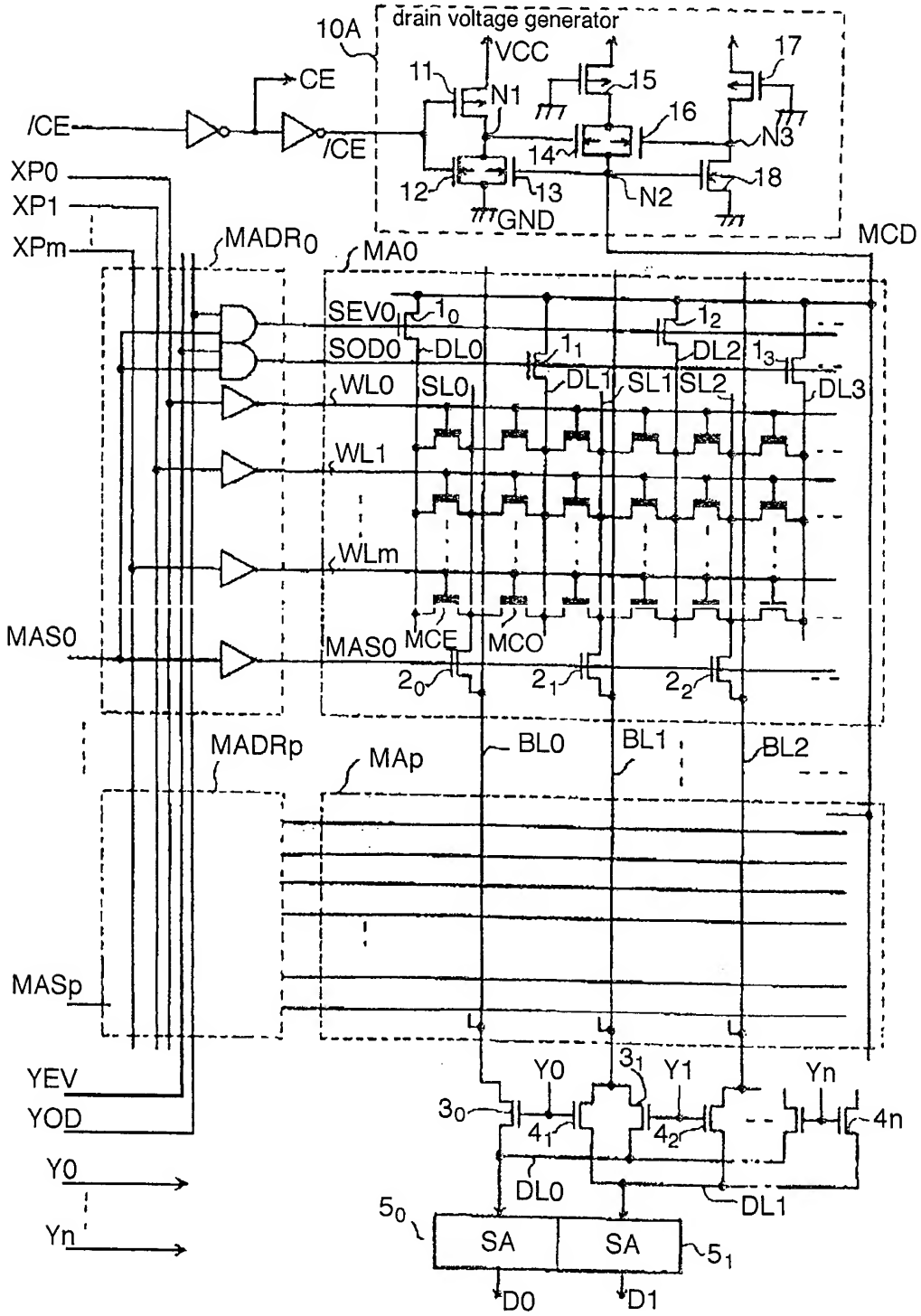

FIG. 2(PRIOR ART)

CONVENTIONAL SEMICONDUCTOR MEMORY DEVICE

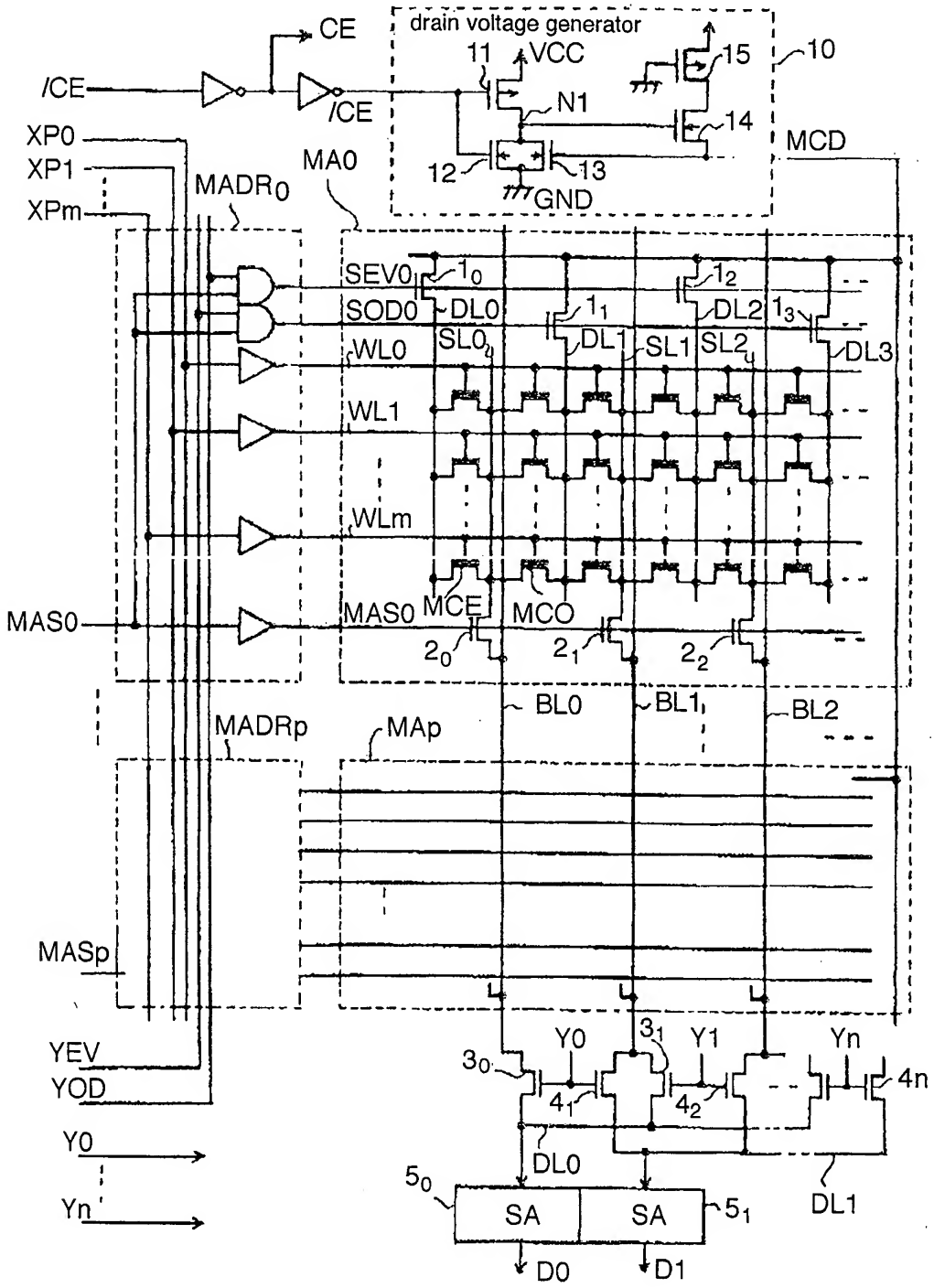

FIG. 3

SEMICONDUCTOR MEMORY DEVICE
ACCORDING TO SECOND EMBODIMENT OF THE INVENTION

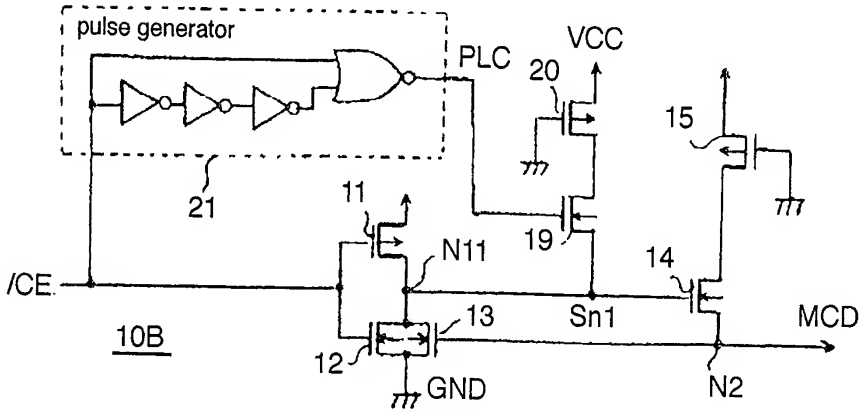

FIG. 4

SIGNAL WAVEFORMS SHOWING
OPERATION OF DRAIN VOLTAGE GENERATOR IN FIG. 3

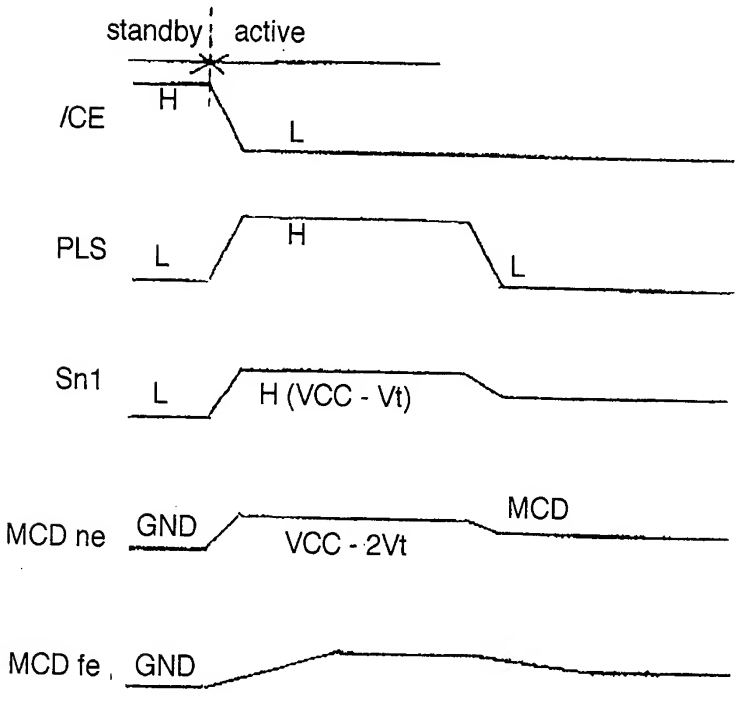

FIG. 5

SEMICONDUCTOR MEMORY DEVICE
ACCORDING TO THIRD EMBODIMENT OF THE INVENTION

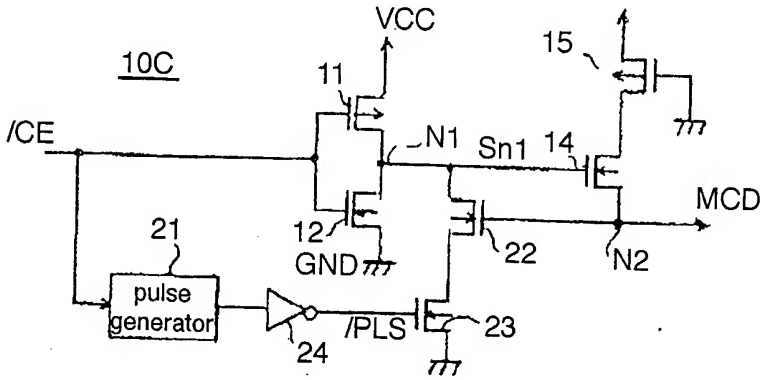

FIG. 6

SIGNAL WAVEFORMS SHOWING
OPERATION OF DRAIN VOLTAGE GENERATOR IN FIG. 5

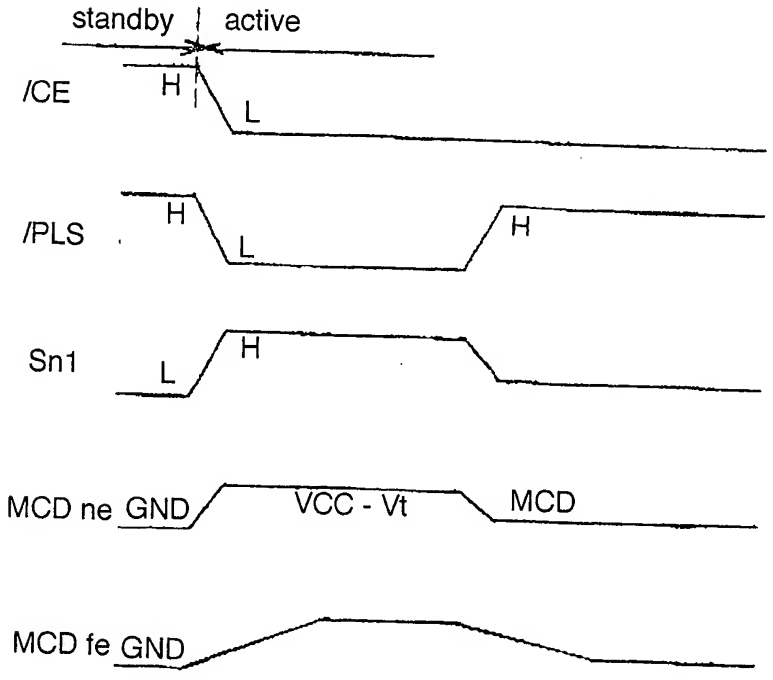

FIG. 7

MEMORY ARRAY ACCORDING
TO FOURTH EMBODIMENT OF THE INVENTION

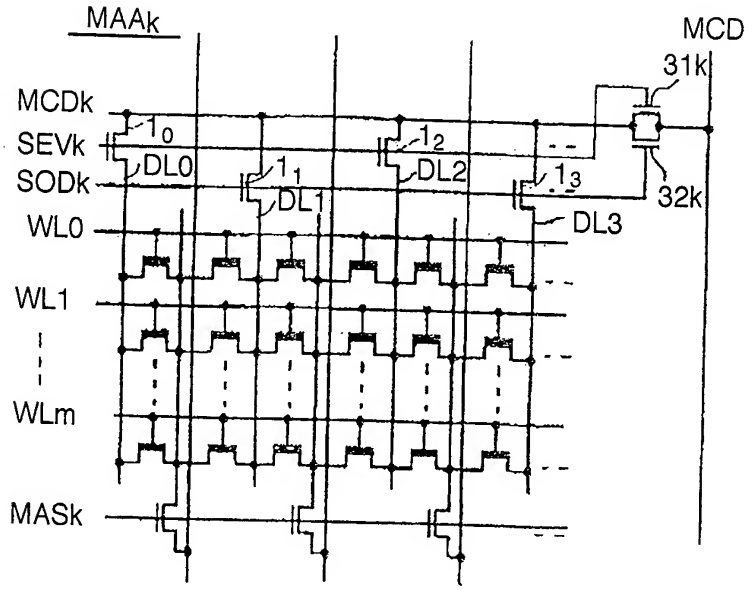

FIG. 8

MEMORY ARRAY ACCORDING
TO FIFTH EMBODIMENT OF THE INVENTION

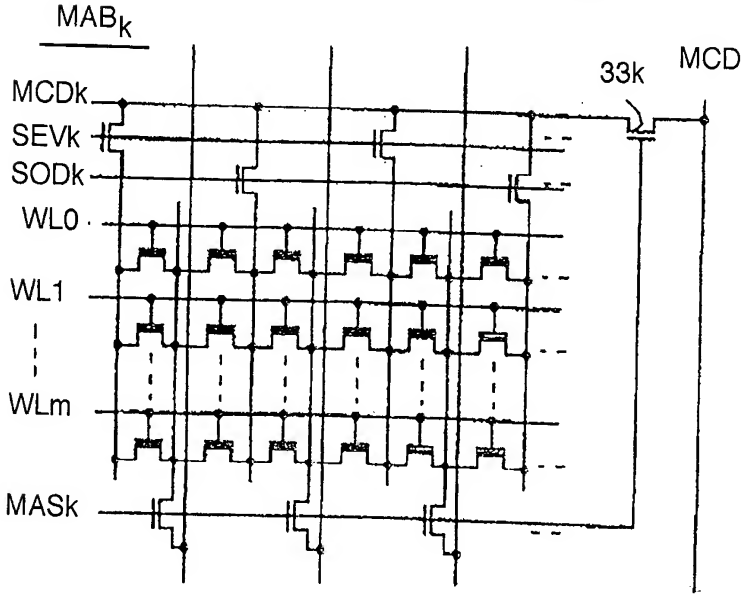

FIG. 9

MEMORY ARRAY ACCORDING
TO SIXTH EMBODIMENT OF THE INVENTION